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EXAMINER

STONER, KILEY SHAWN

ART UNIT PAPER NUMBER

1725

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/053,278

Applicant(s)

BYUN ET AL.

Examiner

Kiley Stoner

Art Unit

1725

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 23-25 is/are allowed.
- 6) ☒ Claim(s) 1-8 and 12-22 is/are rejected.
- 7) ☒ Claim(s) 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3-4.

- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Claim Objections*

Claim 4 is objected to because of the following informalities: In claim 4, line 4 please change "enhanced" to --enhanced pad--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 12-13, 17, 19-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Amagai (6,144,102). The intended use of the instantly claimed article is noted, however, the intended use does not patentably distinguish said claimed article over the prior art. Only the structure of the substrate and the semiconductor chip package have been given patentable weight. Thus, dummy pads and dummy patterns have been considered just pads and patterns, respectively. Dummy pads and dummy patterns have not been structurally limited over ordinary pads and traces. It is the Examiner's position that until electrical connections are formed to the pads all of the pads are dummy pads. In addition, it is inherent that the orientation of the pads (top/bottom) can be changed by flipping the components, thus the pads can be on the top or bottom of the component depending on the orientation.

Amagai et al. teaches an enhanced pad having one or more pads coupled to one or more patterns (Figures 1 and 3; and column 4, line 36-column 5, line 2); said enhanced pads are formed near an outer edge of said substrate (Figures 1 and 3; and column 5, lines 45-63) a solder ball formed on said ball pad (Figures 1 and 3; and column 5, lines 45-63); a substrate, a plurality of enhanced pads each enhanced pad having one or more pads coupled to one or more patterns, a semiconductor chip mounted on and electrically connected to the top surface of the substrate (Figures 1 and 3; and column 4, line 36-column 5, line 2); a molding resin for encapsulating said semiconductor chip (column 1, lines 36-50 and column 2, lines 22-47); ball pads are arranged in a substantially lattice shape on the bottom surface of the substrate (Figures 1 and 3); said enhanced pads comprise a second enhanced pad, and wherein the second enhanced pad comprises a ball pad, a pad, and a pattern connecting said ball pad to said dummy pad (Figures 1 and 3; and column 4, line 36-column 5, line 2); said enhanced pads comprise a third enhanced pad, and wherein the third enhanced pad comprises a plurality of pads and a pattern for connecting said pads to each other (Figures 1 and 3; and column 4, line 36-column 5, line 2); said solder balls are all approximately the same size (Figures 1 and 3; and column 4, line 36-column 5, line 2); arranging ball pads on a bottom surface of the substrate (Figures 1 and 3; and column 4, line 36-column 5, line 2); arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising at least one pad coupled to at least one pattern (Figures 1 and 3; and column 4, line 36-column 5, line 2); arranging said enhanced pads further comprises arranging said enhanced pads near sides of the

substrate; one or more of said enhanced pads comprise a plurality of patterns (Figures 1 and 3; and column 4, line 36-column 5, line 2).

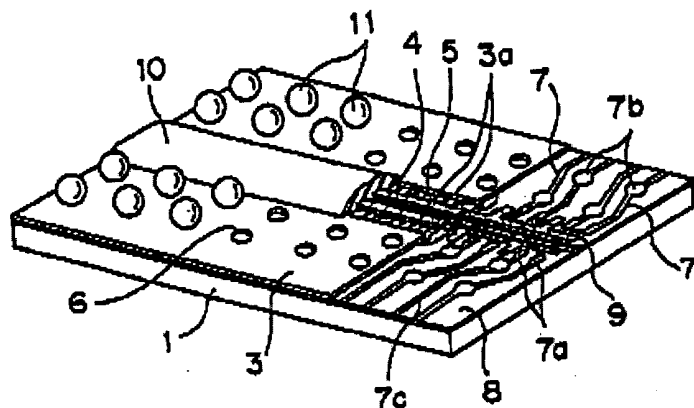


FIG. 1

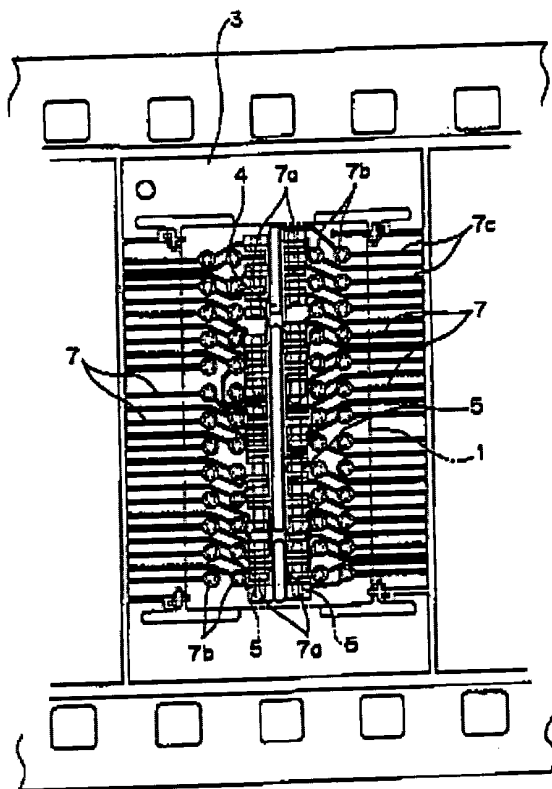


FIG. 3

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 12-14 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kondo et al. (6,303,878 B1). The intended use of the instantly claimed article is noted, however, the intended use does not patentably distinguish said claimed article over the prior art. Only the structure of the substrate and the semiconductor chip package have been given patentable weight. Thus, dummy pads and dummy patterns

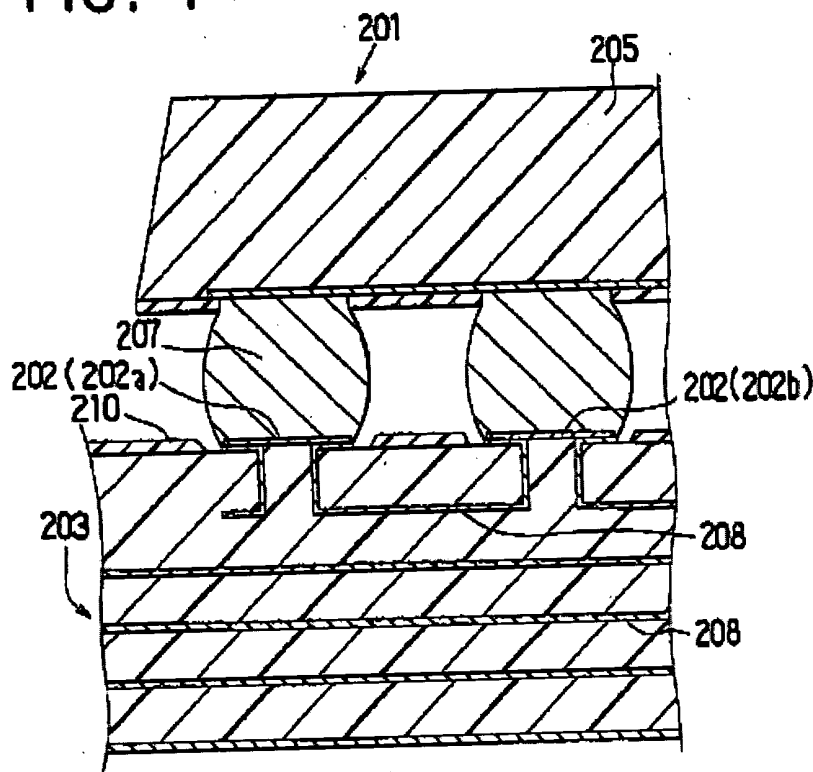
have been considered just pads and patterns, respectively. Dummy pads and dummy patterns have not been structurally limited over ordinary pads and traces. It is the Examiner's position that until electrical connections are formed to the pads all of the pads are dummy pads. In addition, it is inherent that the orientation of the pads (top/bottom) can be changed by flipping the components, thus the pads can be on the top or bottom of the component depending on the orientation.

Kondo et al. teaches an enhanced pad having one or more pads coupled to one or more patterns (Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); said enhanced pads are formed near an outer edge of said substrate (Figure 5); a solder ball formed on said ball pad (abstract and Figures); a substrate, a plurality of enhanced pads each enhanced pad having one or more pads coupled to one or more patterns, a semiconductor chip mounted on and electrically connected to the top surface of the substrate (Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); a molding resin for encapsulating said semiconductor chip (column 4, lines 9-18); ball pads are arranged in a substantially lattice shape on the bottom surface of the substrate (Figures 1 and 3); said enhanced pads comprise a second enhanced pad, and wherein the second enhanced pad comprises a ball pad, a pad, and a pattern connecting said ball pad to said dummy pad (Figure 2; Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); said enhanced pads comprise a third enhanced pad, and wherein the third enhanced pad comprises a plurality of pads and a pattern for connecting said pads to each other (Figure 2; Figure 4, specifically "202a, 202b and

Art Unit: 1725

208"; column 4, lines 27-32; and column 6, lines 52-64); a board, said board comprising enhanced lands corresponding to said enhanced pads and ball lands corresponding to said ball pads, wherein said semiconductor chip package is mounted on said board (Figure 2; Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); said solder balls are all approximately the same size (Figures); a majority of said dummy patterns are arranged parallel to a long side of said substrate (Figure 4, specifically "202a, 202b and 208"); arranging ball pads on a bottom surface of the substrate (Figure 2; Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising at least one pad coupled to at least one pattern (Figure 2; Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64); arranging said enhanced pads further comprises arranging said enhanced pads near sides of the substrate; one or more of said enhanced pads comprise a plurality of patterns (figure 2; Figure 4, specifically "202a, 202b and 208"; column 4, lines 27-32; and column 6, lines 52-64).

**FIG. 4**



Claims 1-8, 12-14 and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (6,242,815 B1). The intended use of the instantly claimed article is noted, however, the intended use does not patentably distinguish said claimed article over the prior art. Only the structure of the substrate and the semiconductor chip package have been given patentable weight. Thus, dummy pads and dummy patterns have been considered just pads and patterns, respectively. Dummy pads and dummy patterns have not been structurally limited over ordinary pads and traces. It is the Examiner's position that until electrical connections are formed to the pads all of the pads are dummy pads. In addition, it is inherent that the orientation of the pads

(top/bottom) can be changed by flipping the components, thus the pads can be on the top or bottom of the component depending on the orientation.

Hsu et al. teaches an enhanced pad having one or more pads coupled to one or more patterns (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); said enhanced pads are formed near an outer edge of said substrate (Figure 5); a solder ball formed on said ball pad (abstract and Figures); a substrate, a plurality of enhanced pads each enhanced pad having one or more pads coupled to one or more patterns, a semiconductor chip mounted on and electrically connected to the top surface of the substrate (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); a molding resin for encapsulating said semiconductor chip (column 1, lines 12-33 and column 3, lines 15-20); ball pads are arranged in a substantially lattice shape on the bottom surface of the substrate (Figure 7); said enhanced pads comprise a second enhanced pad, and wherein the second enhanced pad comprises a ball pad, a pad, and a pattern connecting said ball pad to said dummy pad (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); said enhanced pads comprise a third enhanced pad, and wherein the third enhanced pad comprises a plurality of pads and a pattern for connecting said pads to each other (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); a board, said board comprising enhanced lands corresponding to said enhanced pads and ball lands corresponding to said ball pads, wherein said semiconductor chip package is mounted on said board (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); said solder balls are all approximately the same size (Figures); a majority of said dummy patterns are

arranged parallel to a long side of said substrate (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); arranging ball pads on a bottom surface of the substrate (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising at least one pad coupled to at least one pattern (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44); arranging said enhanced pads further comprises arranging said enhanced pads near sides of the substrate; one or more of said enhanced pads comprise a plurality of patterns (Figure 7, specifically "220c, 220d, 220e"; column 3, lines 14-column 4, line 44).

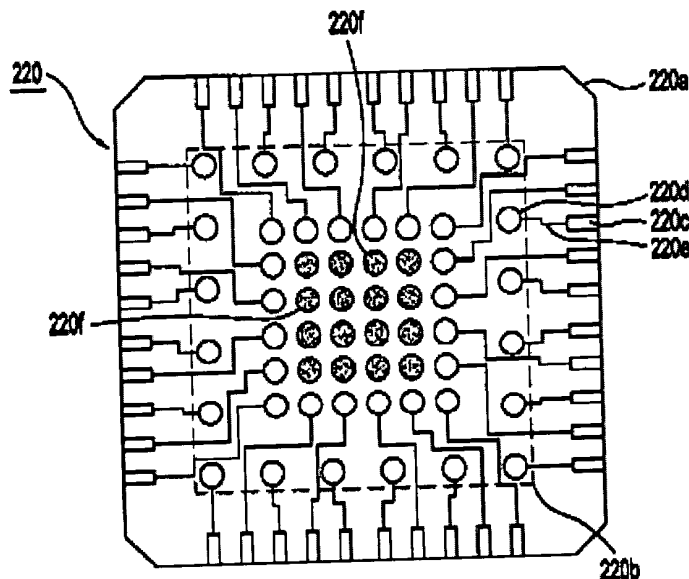


FIG. 7

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo et al. (6,303,878 B1) or Hsu et al. (6,242, 815 B1) as applied to claim 14 above, and further in view of Kasatani (6,492,714 B1). Kondo et al. and Hsu et al. teach all of the limitations of the claims except said semiconductor chip package is mounted on said board by attaching said solder balls formed on said ball pads and said dummy pads of said package to a solder paste coated on said ball lands and said enhanced lands of said board; said solder paste is uniformly formed on said solder balls and said dummy patterns of the enhanced pads by a solder reflow process.

Kasatani et al. teaches said semiconductor chip package is mounted on said board by attaching said solder balls formed on said ball pads and said dummy pads of said package to a solder paste coated on said ball lands and said enhanced lands of said board (column 1, line 63-column 2, line 34 and column 3, lines 20-35). It is inherent that the paste would be uniformly formed on the solder balls and dummy patterns to prevent bridging and short circuits. At the time of the invention it would have been obvious to combine the solder paste reflow method of Kasatani et al. with the semiconductor package of Kondo et al. or Hsu et al. in order to assure that the bumps are electrically connected to the lands and pads during reflow.

***Allowable Subject Matter***

Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 23-25 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest either alone or in combination a semiconductor package as recited by claim 9, particularly the enhanced pads comprise the first enhanced pad, and wherein the first enhanced pad comprises the ball pad, the plurality of dummy pads, and the plurality of dummy patterns configured to connect the ball pad to the dummy pads.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

The prior art of record that is cited as of interest is presented on the form-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiley Stoner whose telephone number is (703) 305-

Application/Control Number: 10/053,278  
Art Unit: 1725

Page 13

0723. The examiner can normally be reached on Monday-Thursday (7:30 a.m. to 6:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on Monday-Friday. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

Kiley Stoner A.U. 1725

*Kiley Stoner* 6-25-03